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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,401	05/11/2007	**Christian Birzer**	I431.167.101	7118

25281 7590 08/06/2008

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

MAIL DATE	DELIVERY MODE
08/06/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/588,401	BIRZER ET AL.	
	Examiner	Art Unit	
	CHRIS C. CHU	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11 - 32* is/are pending in the application.

4a) Of the above claim(s) *24 and 25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11 - 23 and 26 - 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/3/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 11 – 23 and 26 - 32) in the reply filed on May 7, 2008 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 11 – 23 and 26 – 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saeki (U. S. Pub. No. 2003/0,122,237) in view of Sakuyama (U. S. Pat. No. 6,018,462).

Regarding claim 11, Saeki discloses in e.g., Fig. 1 a semiconductor device (the device in e.g., Fig. 1) comprising:

- a semiconductor chip stack (10 and 20; page 1, paragraph 0004, lines 1 and 2) on a rewiring plate (30; page 1, paragraph 0004, line 3), the underside of the rewiring plate (30) forming the underside of the semiconductor device (the device in e.g., Fig. 1);
- an external contact area (the area where the external pads 33 are formed) having a plurality of external contact area (33; page 1, paragraph 0006, lines 6 and 7) regions which are physically separate from one another being arranged on the underside (see e.g., Fig. 1);

- the individual external contact area (33) regions being assigned to the individual semiconductor chips (10 and 20) in the semiconductor chip stack (10 and 20; see e.g., Fig. 1).

Saeki does not disclose a common external contact. Sakuyama teaches in e.g., Fig. 1 the regions of an individual external contact area (4; column 2, line 38) being electrically connected via a common external contact (9; column 3, line 6). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the common external contact of Sakuyama onto the regions of the individual external contact area of Saeki as taught by Sakuyama to reduce unnecessarily occupying the substrate surface area and the reduction of the size of the substrate (column 3, lines 18 – 20).

Regarding claim 12, Saeki discloses in e.g., Fig. 1 the rewiring plate (30) comprising, on its top side, a rewiring structure (32; page 2, paragraph 0025, line 5) which comprises, in the center of the rewiring plate (30), contact pads (32 in the middle that are connected to the chip 10) for connecting a semiconductor chip (10) to flip-chip contacts (see e.g., Fig. 1) and comprises, in the edge region, contact pads (32 in the edge that are connected to the chip 20) for bonding connections (43; page 2, paragraph 0027, line 7) to a stacked semiconductor chip (see e.g., Fig. 1).

Regarding claim 13, Saeki discloses in e.g., Fig. 1 the rewiring plate (30) comprising, in the center of its top side, a rewiring structure (32) for fitting the rear side of a lower semiconductor chip (10) and comprises, in the edge regions, contact pads (32 in the edge that are connected to the chip 20) for bonding connections (43) to top sides of the stacked semiconductor chips (see e.g., Fig. 1).

Regarding claim 14, Saeki discloses in e.g., Fig. 1 the rewiring plate (30) comprising through-contacts via (34) which the contact pads (32) on the top side of the rewiring plate (30) are connected to the external contact area regions on the underside of the rewiring plate (30; see e.g., Fig. 1).

Regarding claim 15, Saeki discloses in e.g., Fig. 1 the rewiring plate (30) comprising rewiring lines (34) which connect the external contact area regions to the contact pads (32; see e.g., Fig. 1).

Regarding claim 16, Saeki discloses in e.g., Fig. 1 the semiconductor chips (10 and 20) of the semiconductor device comprising, on their active top sides, contact areas which are connected, via flip-chip contacts (13) and/or bonding connections (43), to the contact pads (32) on the top side of the rewiring plate (30; see e.g., Fig. 1).

Regarding claim 17, Saeki discloses in e.g., Fig. 1 the semiconductor chip stack (10 and 20) on the rewiring plate (30) being embedded in a plastic composition (44; page 2, paragraph 0027, line 11 and see e.g., Fig. 1).

Regarding claim 18, Saeki discloses in e.g., Fig. 1 a panel (the printed wiring board; page 1, paragraph 0006, line 12) which comprises device positions which are arranged in rows and columns and have semiconductor devices of claim 11 (page 1, paragraph 0006).

Regarding claim 19, Saeki discloses in e.g., Fig. 1 a semiconductor device (the device in e.g., Fig. 1) comprising:

- a semiconductor chip stack (10 and 20) on a rewiring plate (30; see e.g., Fig. 1), the underside of the rewiring plate (30) forming the underside of the semiconductor device (see e.g., Fig. 1);

- an external contact area (the area where the external pads 33 are formed) having a plurality of external contact area regions (33) which are physically separate from one another being arranged on the underside (see e.g., Fig. 1);
- the individual external contact area regions (33) being assigned to the individual semiconductor chips (10 and 20) in the semiconductor chip stack (see e.g., Fig. 1); and
- wherein the rewiring plate (30) comprises, on its top side, a rewiring structure (32) which comprises, in the center of the rewiring plate (30), contact pads (32 in the middle that are connected to the chip 10) for connecting a semiconductor chip (10) to flip-chip contacts (13; see e.g., Fig. 1) and comprises, in the edge region, contact pads (32 in the edge that are connected to the chip 20) for bonding connections (43) to a stacked semiconductor chip (10 and 20; see e.g., Fig. 1), and wherein the rewiring plate (30) comprises through-contacts via (34) which the contact pads (32) on the top side of the rewiring plate (30) are connected to the external contact area regions (33) on the underside of the rewiring plate (30; see e.g., Fig. 1).

Saeki does not disclose a common external contact. Sakuyama teaches in e.g., Fig. 1 the regions of an individual external contact area (4; column 2, line 38) being electrically connected via a common external contact (9; column 3, line 6). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the common external contact of Sakuyama onto the regions of the individual external contact area of Saeki as taught by Sakuyama to reduce unnecessarily occupying the substrate surface area and the reduction of the size of the substrate (column 3, lines 18 – 20).

Regarding claim 20, Saeki discloses in e.g., Fig. 1 the rewiring plate (30) comprising rewiring lines (34) which connect the external contact area regions to the contact pads (32; see e.g., Fig. 1).

Regarding claim 21, Saeki discloses in e.g., Fig. 1 the semiconductor chips (10 and 20) of the semiconductor device comprising, on their active top sides, contact areas which are connected, via flip-chip contacts (13) and/or bonding connections (43), to the contact pads (32) on the top side of the rewiring plate (30; see e.g., Fig. 1).

Regarding claim 22, Saeki discloses in e.g., Fig. 1 the semiconductor chip stack (10 and 20) on the rewiring plate (30) being embedded in a plastic composition (44; see e.g., Fig. 1).

Regarding claim 23, Saeki discloses in e.g., Fig. 1 the rewiring plate (30) comprising, on its top side, a rewiring structure (32) which comprises, in the center of the rewiring plate, contact pads (32) for connecting a semiconductor chip (10) to flip-chip contacts (see e.g., Fig. 1) and comprises, in the edge region, contact pads (32) for bonding connections (43) to a stacked semiconductor chip (10 and 20; see e.g., Fig. 1).

Regarding claim 26, Saeki discloses in e.g., Fig. 1 a semiconductor device (the device in e.g., Fig. 1) comprising:

- a semiconductor chip stack (10 and 20) on a rewiring plate (30; see e.g., Fig. 1), the underside of the rewiring plate (30) forming the underside of the semiconductor device (see e.g., Fig. 1);
- means for providing an external contact area (the area where the external pads 33 are formed) having a plurality of external contact area regions (33) which are physically separate from one another being arranged on the underside (see e.g., Fig. 1);

- the individual external contact area regions (33) being assigned to the individual semiconductor chips (10 and 20) in the semiconductor chip stack (10 and 20; see e.g., Fig. 1).

Saeki does not disclose a common external contact. Sakuyama teaches in e.g., Fig. 1 the regions of an individual external contact area (4; column 2, line 38) being electrically connected via a common external contact (9; column 3, line 6). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the common external contact of Sakuyama onto the regions of the individual external contact area of Saeki as taught by Sakuyama to reduce unnecessarily occupying the substrate surface area and the reduction of the size of the substrate (column 3, lines 18 – 20).

Regarding claim 27, Saeki discloses in e.g., Fig. 1 the rewiring plate (30) comprising, on its top side, a rewiring structure (32) which comprises, in the center of the rewiring plate (30; see e.g., Fig. 1), contact pads (32) for connecting a semiconductor chip (10) to flip-chip contacts (13; see e.g., Fig. 1) and comprises, in the edge region, contact pads (32) for bonding connections (43) to a stacked semiconductor chip (10 and 20; see e.g., Fig. 1).

Regarding claim 28, Saeki discloses in e.g., Fig. 1 the rewiring plate (30) comprising, in the center of its top side, a rewiring structure (32) for fitting the rear side of a lower semiconductor chip (10) and comprises, in the edge regions, contact pads (32) for bonding connections (43) to top sides of the stacked semiconductor chips (10 and 20; see e.g., Fig. 1).

Regarding claim 29, Saeki discloses in e.g., Fig. 1 the rewiring plate (30) comprising through-contacts via (34) which the contact pads (32) on the top side of the rewiring plate (30) are connected to the external contact area regions (33) on the underside of the rewiring plate (30;

see e.g., Fig. 1).

Regarding claim 30, Saeki discloses in e.g., Fig. 1 the rewiring plate (30) comprising rewiring lines (34) which connect the external contact area regions (33) to the contact pads (32; see e.g., Fig. 1).

Regarding claim 31, Saeki discloses in e.g., Fig. 1 the semiconductor chips (10 and 20) of the semiconductor device comprising, on their active top sides, contact areas (32) which are connected, via flip-chip contacts (13) and/or bonding connections (43), to the contact pads (32) on the top side of the rewiring plate (30; see e.g., Fig. 1).

Regarding claim 32, Saeki discloses in e.g., Fig. 1 the semiconductor chip stack (10 and 20) on the rewiring plate (30) being embedded in a plastic composition (44; see e.g., Fig. 1).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tamaki et al., Ball, Shizuno, Egawa, Nakayama et al., and Dotta et al. disclose a stacked semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRIS C. CHU whose telephone number is (571)272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Sunday, August 03, 2008